

Abstract of the Disclosure

A method of identifying faulty programmable interconnect resources of a field programmable gate array (FPGA) may be carried out during manufacturing testing and/or during normal on-line operation. The FPGA resources are configured into a working area and a self-testing area. The working area maintains normal operation of the FPGA throughout on-line testing. During manufacturing testing, the working area may be replaced with additional self-testing areas or the self-testing area extended to include the entire FPGA. Within the self-testing area, programmable interconnect resources of the FPGA are grouped and comparatively tested for faults. Upon the detection of one or more faults within a group of programmable interconnect resources, the group of resources is subdivided for further comparative testing in order to minimize a region of the group of resources including the fault for each fault. Once the region of the group of resources which includes the fault is minimized, the wires within the minimized region are comparatively tested in order to determine which wire includes the faulty resource or resources. Once the wire which includes the faulty resource is determined, a variety of testing configurations may be utilized to identify the faulty resource within the wire. After testing the programmable interconnect resources in the initial self-testing area, the FPGA is reconfigured such that a portion of the working area becomes a subsequent self-testing area and at least a portion of the initial self-testing area replaces that portion of the working area. In other words, the self-testing area roves around the FPGA repeating the steps of testing and reconfiguring until the entire FPGA has undergone testing and its faulty programmable interconnect resources identified.

0994299-112601